WHAT IS CLAIMED IS:

1. A process for the fabrication of integrated resistive elements with protection from silicidation, comprising:

delimiting at least one active area in a semiconductor substrate; and

forming at least one resistive region having a pre-set resistivity in said active area;

forming a delimitation structure that delimits said resistive region on top of said active area; and

providing salicidation protective elements which extend within said delimitation structure and cover said resistive region.

2. The process according to claim 1, wherein forming said delimitation structure comprises making delimiters having portions set facing one another.

3. The process according to claim 2, wherein forming said resistive region comprises implantation of a dopant species in said active area between said delimiters.

4. The process according to claim 1, wherein making protective elements comprises:

depositing a dielectric layer covering said delimitation structure and said resistive region; and

anisotropically etching said dielectric layer.

5. The process according claim 4, wherein, during anisotropically etching, said dielectric layer is completely removed above said delimitation structure and is partially removed above said resistive region.

6. The process according to claim 4, wherein said dielectric layer has a thickness of at least one half of a distance between opposed delimiters defining the delimiting structure.

7. The process according to claim 6, wherein said delimiters have a height of approximately one half of said distance.

8. The process according to claim 4, wherein said dielectric layer is made of a material selected in the group consisting of: silicon dioxide, silicon nitride, and silicon oxynitride.

9. The process according to claim 1, wherein said delimitation structure is made of polysilicon.

10. The process according to claim 1, wherein forming said delimitation structure precedes forming said resistive region.

11. A semiconductor wafer comprising:

at least one active area;

at least one resistor having a resistive region obtained within said active area; and

a delimitation structure set on top of said active area to delimit said resistive region.

12. The wafer according to claim 11, wherein said delimitation structure is made of a material used in the semiconductor industry.

13. The wafer according to claim 12, wherein said delimitation structure is made of a material selected from a group consisting of a dielectric, a semiconductor and a metal.

14. The wafer according to claim 12, wherein said delimitation structure is made of polysilicon.

15. The wafer according to claim 11, characterized by comprising protective elements which extend within said delimitation structure and coat said resistive region.

16. The wafer according to claim 15, wherein said protective elements are made of a dielectric material.

17. An integrated device comprising:

a semiconductor body;

at least one active area on the semiconductor body;

at least one resistor having a resistive region within said active area;

a delimitation structure set on top of said active area to delimit said resistive region.

18. The integrated device according to claim 17, wherein said delimitation structure is made of a material used in the semiconductor industry.

19. The integrated device according to claim 18, wherein said delimitation structure is made of a material selected from a group consisting of a dielectric, a semiconductor and a metal.

20. The integrated device according to claim 18, wherein said delimitation structure is made of polysilicon.

21. The integrated device according claim 17, characterized by comprising protective elements which extend within said delimitation structure and coat said resistive region.

22. The integrated device according to claim 21, wherein said protective elements are made of a dielectric material.

23. A process for integrated circuit fabrication, comprising:

defining an active area in a semiconductor substrate;

forming a resistive region having a pre-set resistivity in the active area;

forming a polysilicon structure which delimits the resistive region;

depositing a protective layer over the polysilicon structure and resistive region;

etching the protective layer back to expose the polysilicon structure without uncovering the resistive region; and

saliciding the exposed polysilicon structure without affecting the pre-set resistivity in the active area.

24. The process according to claim 23, wherein forming the polysilicon structure comprises making opposed delimiters having portions set facing one another.

25. The process according to claim 24, wherein forming said resistive region comprises implantation of a dopant species in said active area between said delimiters.

26. The process according to claim 23, wherein the protective layer is a dielectric layer and the etching is anisotropic.

27. The process according claim 23, wherein the etching of the protective layer completely removes the layer above the polysilicon structure and partially removes the layer above the resistive region.

28. The process according to claim 23, wherein the protective layer has a thickness of at least one half of a distance between opposed delimiters defining the polysilicon structure.

29. The process according to claim 28, wherein the opposed delimiters each have a height of approximately one half of said distance.

30. An integrated circuit fabricated using the method of claim 23.

31. A semiconductor wafer fabricated using the method of claim 23.